CMOS Based Atom Chips for Sensor Applications

Ph. Neumann[1], A. Nemecek[1] and C. Koller[1,2]
1. Department for Micro- and Nanosystems, University of Applied Sciences Wiener Neustadt, Austria
2. School of Physics and Astronomy, University of Nottingham, Nottingham, UK

Introduction: Magnetically trapped ultra-cold atoms are promising candidates for the realization of quantum technological applications such as sensing and simulation. Integration of this technique is possible using the fields generated by currents running in on-chip micro-fabricated wires. Using the magnetic dipole interaction

$$V = -\vec{\mu}\vec{B} = -m_F g_F \mu_B \left|\vec{B}\right| \qquad (1)$$

,where g_F denotes the Landé factor of the hyperfine state, m_F the magnetic quantum number and μ_B the Bohr magneton. One sees that in case of $\mu<0$ the atoms are drawn to the minimum of the magnetic field. In the following we will investigate using Comsol, whether chips fabricated using standard CMOS fabrication techniques can produce sufficient magnetic field strengths in order to act as atomic traps for ultra-cold atoms.

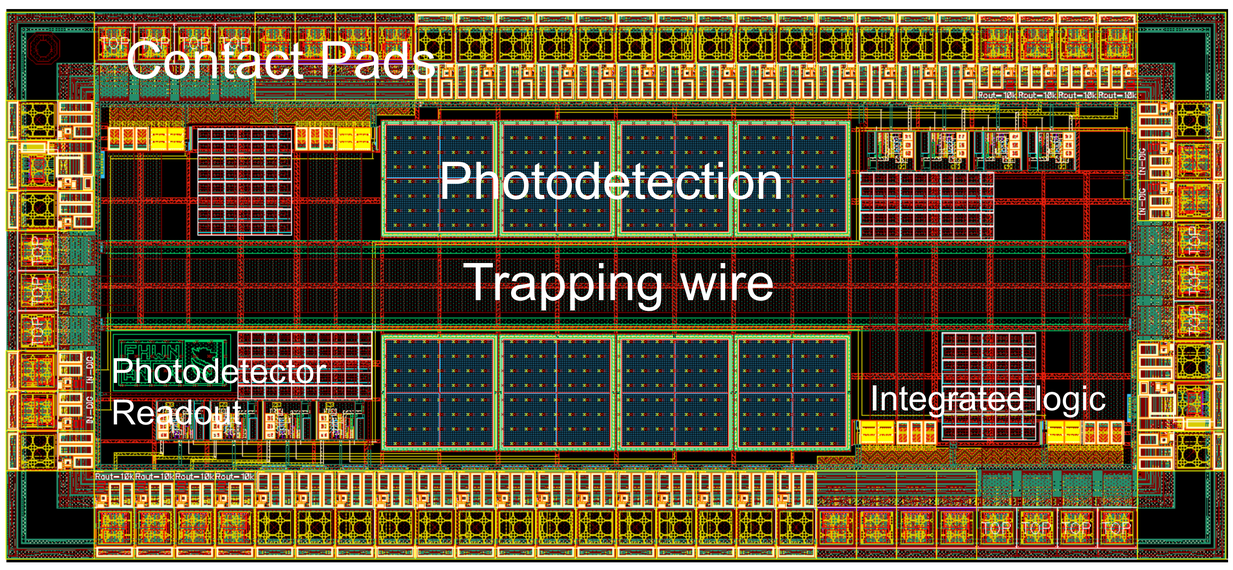

Figure 1. Integrated atom trap layout in CMOS technology

Computational Methods: Figure 1 shows the layout for the atom chip, which is currently fabricated using a submicron CMOS process [2]. We use Comsol's magnetic fields interface in order to simulate the transvers confinement over the chip. The currents used are set along the maximum safe values that can be achieved using the top and analog metal layers according to specification. The minimum is formed by using these wires and adding an offset field B_{off} of ~50G in x-direction generated by external coils. To determine the transvers confinement a 2D simulation using the geometry shown in figure 2 will suffice. The resulting trap depth is usually expressed in the maximum temperature, that is allowed to be trapped by using

$$T = V/k_B \qquad (2)$$

Trap depth on the order of mK are usually required to ensure lifetimes on the order of seconds [1,3].

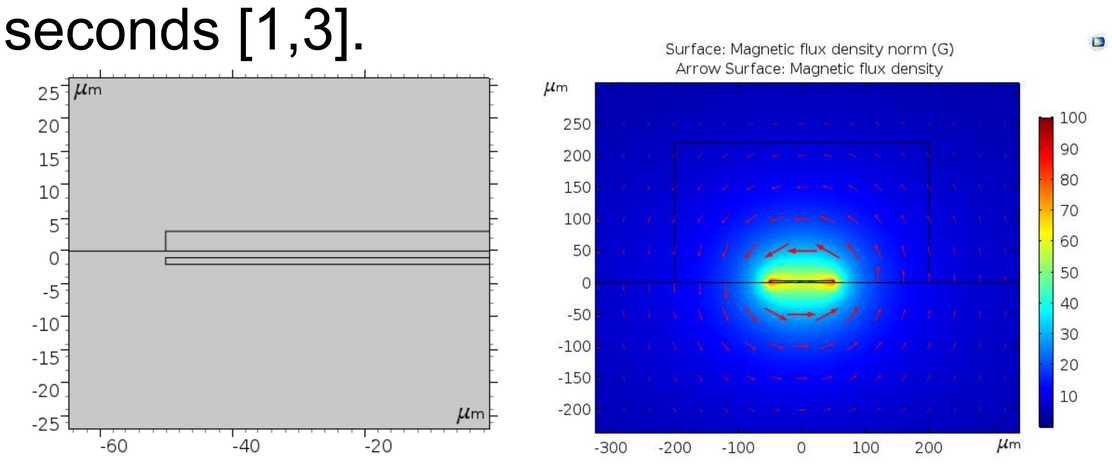

Figure 2. (Left) Left half of geometry. The upper half consists of air, the lower of silicon. Top and analog metal layer wires of 100μm width are visible in between. (Right) Field generated by a single on chip wire

Results: Using formula 1&2 one can obtain directly the depth of the trap for Rb87 atoms in the |2,2> state as well as the shift of the trap position when the total current is altered. (see figure 3)

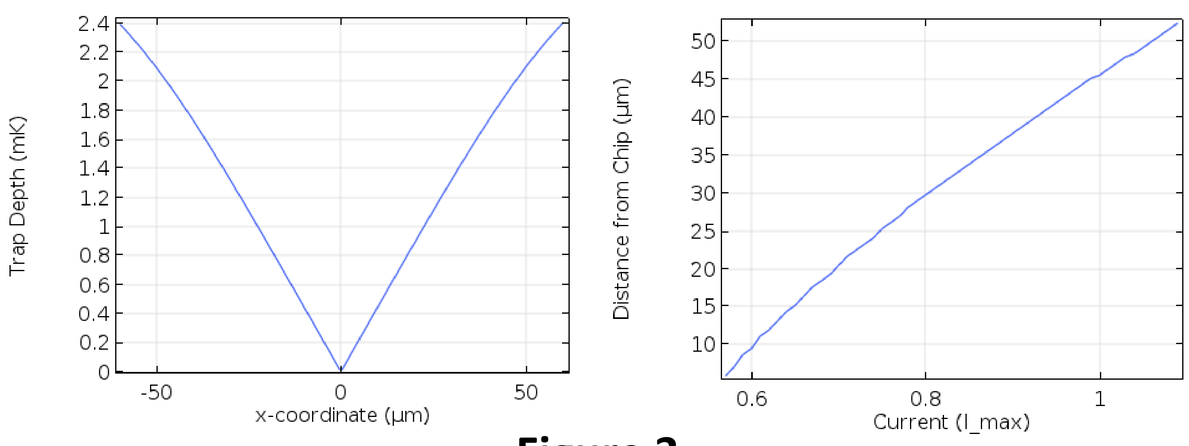

Figure 3.
Generated Potential (left), Central Trap Position (right)
Both generated with an offset field of 50G

Conclusions: These basic simulations show that atom chip based systems should be realizable utilizing CMOS technology. This will open the pathway to implement cold atom sensor technology [3] using large scale manufacturing. Extending the simulation to full 3D will in addition further studies of the CMOS atom chip such as thermal properties.

References:

1. R. Folman et al. , "Microscopic atom optics: From wires to an atom chip , Advances in Atomic, Molecular, and Optical Physics, 48, 263-356 (2002)
2. www.ams.com Sub-micron process (confidental)
3. M. Keil et al., "Fifteen years of cold matter on the atom chip", Journal of Modern Optics, 63, 1840 - 1885 (2016)

Excerpt from the Proceedings of the 2017 COMSOL Conference in Rotterdam