SOI CMOS Based Transistor Model for Low Power Wireless Sensor Network

Siddhartha Panigrahi[*1], Pradipta Kumar Nanda[*2]
[1]ITER, SOA University, [2]ITER, SOA University
[*1] Department of ECE, ITER, Bhubaneswar, India – 751030, s.panigrahi127@gmail.com
[*2]Department of ECE, ITER, Bhubaneswar, India – 751030, pknanda@soauniversity.ac.in

Abstract: Wireless sensor nodes have finite energy and hence limited lifetime. It is well known that the transceiver section consumes maximum energy while transmitting data to other nodes. Low Noise Amplifier (LNA) is known to consume major chunk of power. In this paper attempts have been made to reduce the power consumed by LNA by proposing two SOI CMOS based transistor topologies that have reduced drain current and have reduced power consumption. The proposed models namely Hole model and Sandwich model have been implemented through COMSOL 3.5. It has been found that these two models resulted in reduced drain current as compared to SOI CMOS.

Keywords: SOI CMOS, Wireless sensor nodes, LNA, COMSOL

1. Introduction

Wireless sensor network has been extensively applied in a wide variety of areas such as defense, agriculture, transportation etc [1,5]. The major challenge in those networks is the finite energy of the sensor node which is by and large engaged in transmitting and receiving data. It is known that substantial amount of energy is consumed in transmitter portion. The constituent unit of the transmitter i.e., LNA consumes the bulk of power [2,3].

Vivian Ma [2] has reviewed the basic circuit issues of the SOI CMOS and has compared the performance of SOI CMOS based RF circuits with that of Bulk CMOS circuits. Recently Chen et al [3] has proposed the design of low noise chopper amplifier for special applications such as down-hole-drilling where the data acquisition and transmission becomes a horrendous task. Besides Sanz et al [4] has proposed a novel self-cascode of two fully depleted SOI CMOS which has been found to have low output conductance. They have also proposed Graded channel SOI CMOS MOSFET that has improved performance in saturation. The RF application of fully depleted SOI CMOS has been proposed by Ichikawa et al [5] where it has been found that the proposed one has superior performance at GHz frequency range as compared to that of bulk CMOS. Otis [6] in his doctoral dissertation has addressed the issue of designing and implementing the low power CMOS technology for wireless sensor network applications.

To achieve minimized power consumption SOI CMOS is widely used rather than the traditional CMOS. It has been reported in the literature that SOI CMOS based circuits consume low power and have low junction capacitance [1,2,5]. This in turn enhances the switching speed of the sensor node.

In this research attempts have been made to reduce the internal capacitance as well as the drain current which in turn reduce the power by modifying SOI CMOS structure. The advantage of SOI CMOS is that it has a buried oxide layer above the silicon layer and this helps in reducing the capacitance and also in drain current. In order to minimize power consumption, the drain current needs to be minimized and to achieve this two SOI CMOS based topologies have been proposed in this paper.

2. Problem Statement

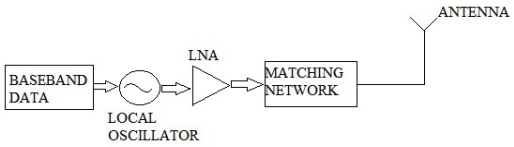

Figure 1. A simple OOK transmitter

Figure 1 shows the schematic block diagram of transmitter section of a wireless sensor node. Most of the power is known to be consumed by the Low Noise Amplifier (LNA) of the node. This is evident from the data provided in Table 1. As seen from the table, LNA consumes 48% of the total power and hence the low power design of LNA would reduce the power consumption of the sensor node appreciably. The

LNA consists of some active and passive components as shown in Figure 2. Since the passive RLC components have been fixed, the only choice left is to redesign the active component that is the transistor to reduce the power consumption.

COMPONENTS	POWER CONSUMPTION
Modulator	2%
Frequency Synthesizer	40%
LNA	48%
Mixer	10%

Table 1. Power consumption in the transmitter section

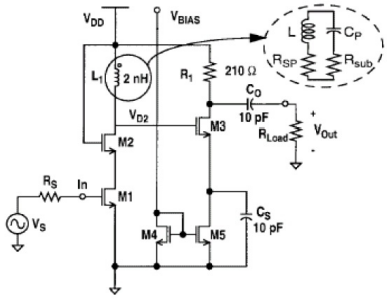

Figure 2. Schematics of a 4GHz amplifier

Usually the transistors are without an oxide layer, but SOI CMOS based design offers to create fully depleted and partially depleted regions for the flow of source to drain current. Therefore we have attempted different topologies of the BOX layer to reduce the leakage current and in turn reduce the source to drain current. Besides the internal capacitance along with the external capacitance determine the switching speed of the transistor. Since SOI CMOS has the advantage of reducing the junction capacitance, the proposed topologies will have reduced capacitance and hence enhanced switching speed.

3. Proposed Topologies

In this research we have proposed two different topologies of SOI CMOS in order to achieve reduced drain current as well as reduced internal capacitance to enhance the switching speed. The buried oxide layer has been appropriately designed to allow the depletion layer to be suitably formed to reduce the drain current. The first proposed one is the hole model and the other one is the sandwiched model.

3.1 Hole Model

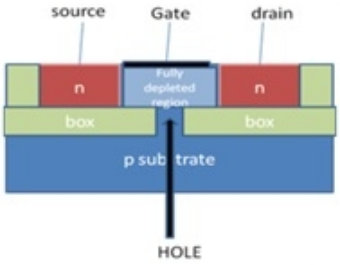

Figure 3. Hole Model

As shown in Figure 3, in the Hole model we have one layer of buried oxide with a hole appropriately chosen to have small leakage current. The size of the hole has been fixed by trial and error.

3.1 Sandwich Model

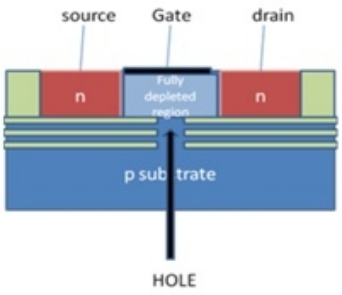

Figure 4. Sandwich Model

Analogously the sandwich model also provides varied depletion layer to have small leakage current. But the oxide layers are separated to provide efficient heat dissipation. This can be viewed as providing multilayer boxes to achieve different strata depletion and also to reduce leakage.

These two topologies have been implemented in the COMSOL version 3.5 and have been found to have very much reduced drain current as compared to that of bulk CMOS. Since SOI CMOS reduces the junction capacitances, these modified topologies are expected to reduce the junction capacitance hence enhance switching speed.

4. Use of COMSOL

The proposed topologies have been simulated and analyzed through COMSOL 3.5 software. The MOS model present in the model library has been reused to simulate the proposed topologies. All the material parameters for CMOS have been kept same as shown in the table below.

NOTATION	VARIABLE	VALUE
n_i(Si)	ni_Si	$1.46 \cdot 10^{10}$ cm^{-3} (T = 300K)
ε_r(Si)	epsilonr_Si	11.8
ε_r(SiO2)	epsilonr_Si	4.2
μ_n(Si)	mun	1000 cm^2/Vs (low concentration)
μ_p(Si)	mup	500 cm^2/Vs (low concentration)
$D_n = \mu_n(Si) \frac{kT}{q}$	Dn	20.7 cm^2/s
$D_p = \mu_p(Si) \frac{kT}{q}$	Dp	5.17 cm^2/s
τ_n	taun	~0.1 μs
τ_p	taup	~0.1 μs
E_G(Si)	Eg_Si	1.08 eV
χ_{Si}	X_Si	4.0 eV
χ_{SiO2}	X_SiO2	0.3 eV
χ_{poly}	X_poly	4.2 eV

Table 2. Parameters for MOS transistor

4. Results and Discussions

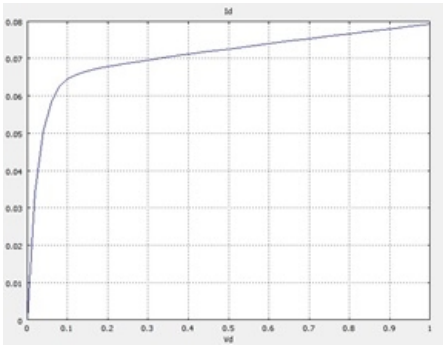

Figure 5. V_d – I_d characteristics of bulk CMOS

The above mentioned two topologies have been simulated using COMSOL using the default parameters available in the library. We have also simulated the bulk CMOS for comparison with the SOI CMOS that has also been implemented in COMSOL. In case of SOI CMOS the BOX layer is all through the channel without any hole or other paths for current. The output (V_d - I_d) has been shown in Figure 5. As observed from Figure 5, the drain current increases from 0 to 65 mA within 0.1 Volt of V_d and thereafter further to 80 mA at 1 Volt of V_d. The result obtained from SOI CMOS is shown in Figure 6, and it has been found that saturation drain current is 60 mA which is at 0.16 Volt. In case of bulk CMOS the current monotonically increased till 1 Volt of V_d.

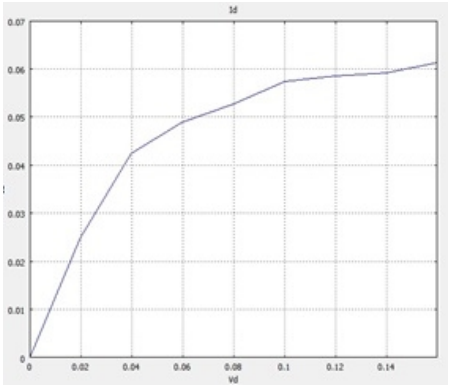

Figure 6. V_d – I_d characteristics of SOI CMOS

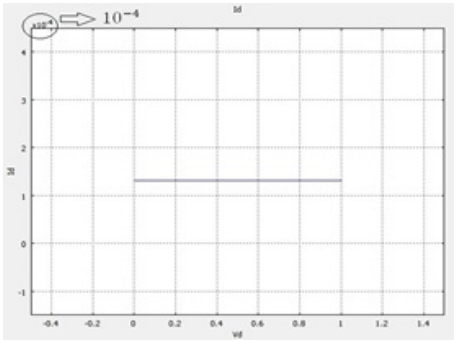

Figure 7. V_d – I_d characteristics of Hole Model

The results obtained for the hole model of the proposed topology is shown in Figure 7 where it may be observed that the drain current rises to around 125 μA with a very small finite voltage and gets to saturation at that value of current. This is maintained till 1 Volt of V_d. As compared to SOI CMOS and bulk CMOS the drain current has reduced almost by three orders from mA to μA and hence will have very much reduced power. Thus the proposed topology can achieve reduced current. Similar observation has been made with Sandwich model and the

corresponding result is shown in Figure 8. The Saturation current is 125 μA which is same as the Hole model. The rise time of the current has been found to be very small. In the Sandwich model drain current is very small at 1 Volt of V_d. Therefore the power consumed will be much lower to bulk CMOS or SOI CMOS.

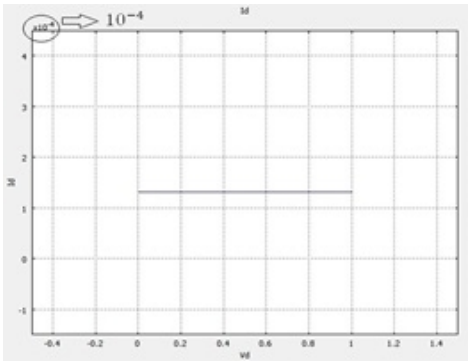

Figure 8. V_d – I_d characteristics of Sandwich Model

5. Conclusion

Two new topologies for SOI CMOS have been proposed with a view to achieve reduced drain current which in turn will result in reduced power consumption. The saturation drain current in the proposed models has been found to be three orders less than those of bulk and SOI CMOS. This has been achieved by controlling the depletion layer with a view to reduce the leakage current. The hole provided by in the BOX has been achieved by trial and error. Further research can be carried out to reformulate as an optimization problem and determine the optimal value of the size of the hole. Since the SOI CMOS has the added feature of reducing the internal capacitance which in turn enhances the switching speed, the proposed SOI CMOS topologies are expected to reduce the capacitance there by enhancing the switching speed.

6. References

1. Takayasu Sakurai et.al, *"Fully-DepletedSOI CMOS circuits and Technology for Ultra-low power Applications"*, pp 23 - 62, Springer, The Netherlands (2006)

2. Vivian Ma et.al, *"SOI vs CMOS FOR ANALOG CIRCUIT"*, Technical Report, University of Toronto

3. Y. Chen et.al, "An SOI-CMOS Low Noise Chopper Amplifier for High Temperature Applications", *Proceedings of IEEE on Integrated Circuits*, pp 240 – 243 (2014)

4. M.T. Sanz et.al, "Self-cascode SOI versus Graded-channel SOI MOS Transistors", *Proceedings of IEEE on Circuits, Devices and Systems*, **Volume 153, No 5**, pp 461-465 (2006)

5. F. Ichikawa, "Fully depleted SOI process and device technology for RF applications", *Solid-State Electronics*, **Volume 48**, pp 999 – 1006 (2004)

6. Brian Patrick Otis, "Ultra-Low Power Wireless Technologies for Sensor Networks", Ph.D. thesis of UC, Berkeley (2005)