

Analyzing Electromagnetic Modes of Integrated Busbars implemented as Printed Circuit Boards (PCB)

A. Pokryvailo

Spellman High Voltage Electronics Corp.

475 Wireless Blvd, Hauppauge NY 11788, apokryva@spellmanhv.com

Abstract: This report addresses design of a PCB intended for use as a busbar integrated with multiple DC-link (rail) capacitors in a high power inverter. The geometry and current ratings are typical of a 50-kW unit operating at 60 kHz in an intermittent mode.

First, circuit aspects are analyzed. The key points are that a) the rail capacitors, Cr, currents are rich in high harmonics; b) there may be resonances between Cr's and parasitic inductances, especially on high harmonics; c) the fundamental frequency is doubled.

Field simulations are called for to study current sharing between Cr's and current distribution on the board. The analysis is done in frequency domain with AC/DC module. FEA is challenging, mainly because of the huge aspect ratio. This problem can be partially circumvented capitalizing on the fact that the conductors are much thinner than the rest of the geometric entities. With Transient Boundary Conditions (TBC) and Impedance Boundary Conditions (IBC), conductors' bulk is not modeled; only surface currents flow. Cr's are modeled as geometrically small Lumped Elements (LE), presenting L, C connected in series. Capacitive LEs were also modeled in volume, to include their parasitic inductance. Both options showed similar results. With this approach, convergence was good, and simulation time was short. Benchmarking simulations were performed both in 2D and 3D on simplified models to determine simulations accuracy. They showed that losses are typically underestimated by units to tens of percent compared to full volume simulations, depending on the ratio of the layer thickness to skin depth.

PCB simulations in a wide range of frequencies allowed visualization and quantification of Cr's currents, proving existence of resonances at certain frequencies. Higher harmonics may increase losses and distort current sharing, which is best be explored experimentally.

Keywords: Comsol, power inverter, printed circuit board, inductance, skin depth.

1 Introduction

High-power inverters employ one or more low-impedance capacitors to isolate the reservoir filter from high-frequency currents. Such capacitors, which are usually film, are called DC-link, or rail capacitors, Cr. They are mounted as close as possible to the switching devices to minimize spurious overvoltages generated on abrupt current changes by parasitic inductances of connections. The latter usually are discrete or laminated busbars. An overview of common techniques can be found elsewhere (see, e.g., [1] and its references). Busbars can be integrated with Cr's and other components. In this case, an attractive design and manufacturing option is using standard PCB with copper weight 4 oz (0.14-mm thickness) or less to reduce costs. Using thin copper is however a challenge in view of heavy high-frequency currents circulating in the busbars. If multiple Crs are used, an additional problem is current sharing between them. This is where field modeling can yield valuable insight and quantitative information on losses and stresses on Cr's and PCB copper.

FEA is challenging, mainly because of the huge aspect ratio of the order of 1000:1. This problem can be partially circumvented capitalizing on the fact that the conductors are much thinner than the rest of the geometric entities. With Transient Boundary Conditions (TBC) and Impedance Boundary Conditions (IBC), conductors' bulk is not modeled; only surface currents flow [2] (the approach suggested by COMSOL Support). In this way, computational resources are used efficiently. Whereas there is little doubt as to the accuracy of simulation of the current distribution in the PCB plane (conductor surface), error of loss calculation is a murky issue. It is not defined in literature including that of COMSOL (manuals, blogs, etc.). With this in mind, we also performed benchmarking simulations in both 2D and 3D on simplified models to determine loss calculation accuracy. These simulations are transferred to Appendix.

2 Description of physical object; its reduction to simulation model

Figure 1 shows a top view of a 50-kW inverter operating at 60 kHz in an intermittent mode. There are total of 16 pcs of 6-μF capacitors, grouped in pairs which are numbered, shown as brown rectangles, mounted on a two-layer PCB. The switching devices are seen under PCB.

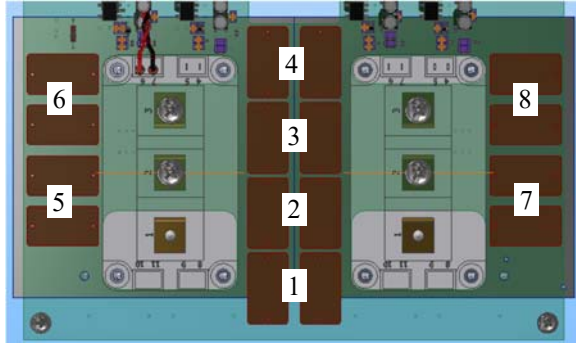


Figure 1. Inverter chassis (half). Switching devices here are 62-mm modules (see, e.g., [4]).

A corresponding simplified circuit model is shown in Figure 2. This is a full-bridge inverter Z1-Z4 fed from a DC source. Current flowing through L34 is virtually a DC current. Only two DC-link capacitors are modeled (C81, C82); they provide high-frequency current. The values of parasitic inductances L35, L36 are chosen rather arbitrarily; they represent geometrical difference in physical connections. Sample waveforms are shown in Figure 3. Of course, they are not sine, and depending on the switching frequency and the L, C values there may be resonances excited, etc. Note that some of the resonances may occur at high harmonics.

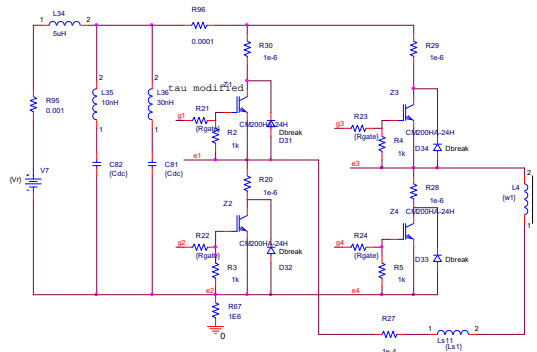


Figure 2. Inverter simulation circuit (PSpice).

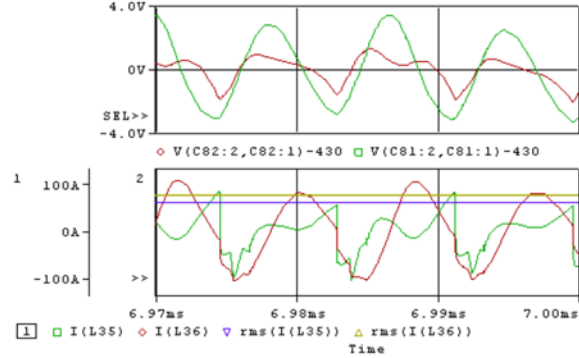


Figure 3. Simulation of circuit fig.1. Ripple on Cr's is shown in top plot, and current through them in bottom plot.

It is clear that the pattern of the currents' flow can be very complex, depending on the switches state. However, analyzing for fundamental frequency, we can simplify the situation assuming that, for instance, Z1, Z4 are closed permanently. Then the load (transformer) in the inverter diagonal can be modeled as a sine current source connected to the rails (top and bottom of PCB). The current source terminals have specific location on the board, namely, 3, 2 of the left and right modules, respectively, if Z1 belongs to the left one. During the next half-period, the current source connects to terminals 3, 2 of the right and left modules, respectively, so actually analysis of one half-period, in terms of fixed geometrical connections, suffices.

After said simplifications, we can transit to building a model for field simulation.

3 Use of COMSOL Multiphysics

The problem was solved using the Magnetic Field interface in frequency domain. The governing subset of Maxwell equations for the frequency domain is shown below:

$$(j\omega\sigma - \omega^2\epsilon_0\epsilon_r)\mathbf{A} + \nabla \times \mathbf{H} = \mathbf{J}_e$$

$$\mathbf{B} = \nabla \times \mathbf{A}$$

where ω is angular frequency, σ is material conductivity, ϵ_0 is permittivity of free space, ϵ_r is relative permittivity, \mathbf{A} is magnetic vector potential, \mathbf{H} is magnetic field, \mathbf{J}_e is current density, and \mathbf{B} is magnetic flux density.

A model in Figure 4 shows a 2-mm-thick board with 0.14-mm copper layers modeled as Transition Boundary Condition (TBC). Using a Lumped Port (LP), a current source injects 150 A into the board

through external wires on whose surface Impedance Boundary Conditions (IBC) are imposed (suggested by Dr. W. Frei). The *volume* of these wires is excluded from simulation; their *surface* is conductive. The connection to the top layer corresponds to the positive terminal 3 of the left module. Connection to the bottom is to terminal 2 of the right module. The current closes via *Lumped Elements* (LE) modeling Cr's. In this model, there are 8pcs, each $2 \times 6 \mu\text{F} = 12 \mu\text{F}$, modeling a pair of Cr's, total 16. They appear as small circles, and physically are cylinders, or "dots", 4-mm-diameter placed between copper plates. It is a crude representation, but probably suitable for finding current division between Cr's.

Comsol allows also a combination of RLC's in LE. We modeled two LE options: pure $C=12 \mu\text{F}$, and L, C connected in series, with $L=15 \text{ nH}$, a value corresponding roughly to that specified by Vishay for 27.5-mm pitch (1 nH/mm, two capacitors in parallel). A series LC connection, rather than parallel, is chosen because the real capacitor impedance tends to a minimum at a certain frequency. Only LC option simulations are reported here.

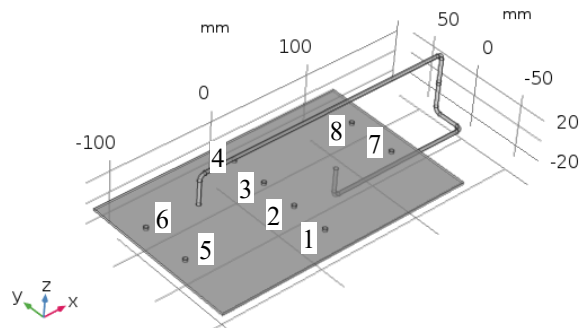


Figure 4. Geometry with LE placement and notation.

We continue with a more sophisticated model (shown later), also representing Cr's as LE, but in volume.

4 Results

Table 1. Capacitors' currents, real part. LC.

	real(LE1)	real(LE2)	real(LE3)	real(LE4)	real(LE5)	real(LE6)	real(LE7)	real(LE8)	sum
freq (Hz)	A								
1.2E+05	18.9	18.9	18.9	18.9	19.1	19.1	18.1	18.0	149.91
2.4E+05	19.8	20.0	20.0	19.5	21.6	21.5	14.0	13.5	149.91
3.0E+05	22.1	22.9	22.6	21.3	32.0	31.8	-0.4	-2.4	149.91
3.3E+05	29.6	31.4	30.4	27.1	-43.8	-50.3	62.7	62.7	149.91
3.6E+05	-6.6	8.6	10.2	-6.5	7.9	22.3	49.8	64.2	149.91
4.2E+05	15.4	14.1	14.3	16.1	13.2	14.1	30.5	32.4	149.91

4.1 Cr's modeled as small cylinders (Figure 4)

Examination of the LE currents Table 1, Table 2 shows that a) real parts sum to 150 A, and imaginary to virtually zero; b) current sharing is good at 120 kHz and below; c) much higher currents flow at resonance, some of them at different phases. The tabulated results are in line with the surface current density plots Figure 5, where it can be seen that at 330 kHz, LE5, LE6, and LE7, LE8 carry very high currents in opposite directions, respectively. We note that although the losses peak at 330 kHz, the LE impedance duly minimizes at 375 kHz where it transits from capacitive to inductive.

It is evident that skin effect is very pronounced in the copper plane: current density on the board edges is much higher than that in its center. (Whatever eddy currents exist in the copper layer *thickness* are ignored by TBC.)

Inductance is not calculated explicitly; it needs to be derived from energy integration. We do not want to include the inductance of connecting wires. With this purpose, an additional volume was introduced artificially – a box enveloping PCB, excluding horizontal wire stretches. The inductances derived from different volumes' integration are tabulated in Table 3. A good part of the inductance calculated from the volume enveloping PCB is that of the vertical parts of the wires ($\sim 1 \text{ nH/mm}$).

Resistive losses are calculated as integral of surface losses accounting for the copper thickness (0.14 mm), excluding losses in wires – see Table 4 summarizing the results for both dot LE and volume LE simulations. Loss calculation error is discussed in Appendices; [2], [3] state that accuracy is quite good.

There is a notable peak at $\sim 330 \text{ kHz}$, slightly below LE resonant frequency of 375 kHz, which is reasonable, because the copper sheets' inductance adds to that of the LE.

Table 2. Capacitors' currents, imaginary part. LC.

	Im(LE1)	Im(LE2)	Im(LE3)	Im(LE4)	Im(LE5)	Im(LE6)	Im(LE7)	Im(LE8)	sum
freq (Hz)	A								
1.20E+05	0.004	0.013	0.022	0.022	0.003	0.022	0.028	0.021	0.135
2.40E+05	-0.053	-0.025	0.006	0.010	-0.122	-0.061	0.150	0.139	0.043
3.00E+05	-0.227	-0.166	-0.085	-0.054	-1.416	-1.324	1.609	1.683	0.019
3.30E+05	-1.327	-1.213	-0.936	-0.731	-198.5	-209.5	200.3	212.0	0.013
3.60E+05	34.416	-34.614	-37.062	31.600	-1.654	1.169	-0.385	6.531	0.000

Table 3. Inductances derived from energy integration on different volumes. Pure C.

freq (Hz)	L, H		
	total volume	PCB only	PCB and box enveloping it
1.20E+05	2.92E-07	7.26E-09	4.67E-08

4.2 Caps (pairs) modeled in volume

The difference from the previous section, where Cr's were modeled as small volumes, is that they are modeled as a body with a length similar to the capacitor pitch Figure 6. This was supposed to introduce the cap inductance without specifying it explicitly. One side of the "handles" with cross-section 4x4 mm is connected to the top, and another to the bottom copper plate. Circular clearings on top provide insulation. It is important to note that LEs specified as capacitances $C=12 \mu\text{F}$ are geometrically the horizontal bars only Figure 7a. LE numbering is the same as in the previous case of dot capacitors Figure 4; handlebars are centered on the dots.

Figure 8 shows surface currents in the selected LE5, at 300 kHz.

Losses Table 4 also peak at a certain frequency, this time at ~300 kHz. General behavior is similar to the "dot" LEs case. A slightly lower resonant frequency corresponds to $L \approx 22 \text{ nH}$, which matches roughly the handlebar inductance estimated from its geometry. (By "handlebars" we mean the horizontal, long part of the "handles"; physical parts are much bulkier, hence have lower inductance.) The nature of the resonance in this case, where the inductance is "built-in", is ambiguous. One may argue that it is the same series resonance as with the LC LEs, or parallel, when individual capacitance and inductance currents can be huge, but their algebraic sum is limited.

Integration of electric field along the LE edges Figure 7b results in the voltage across LE. It goes to a minimum of ~0.1 V at 330 kHz Figure 7 indicating to a series resonance. Anyway, the losses are very similar

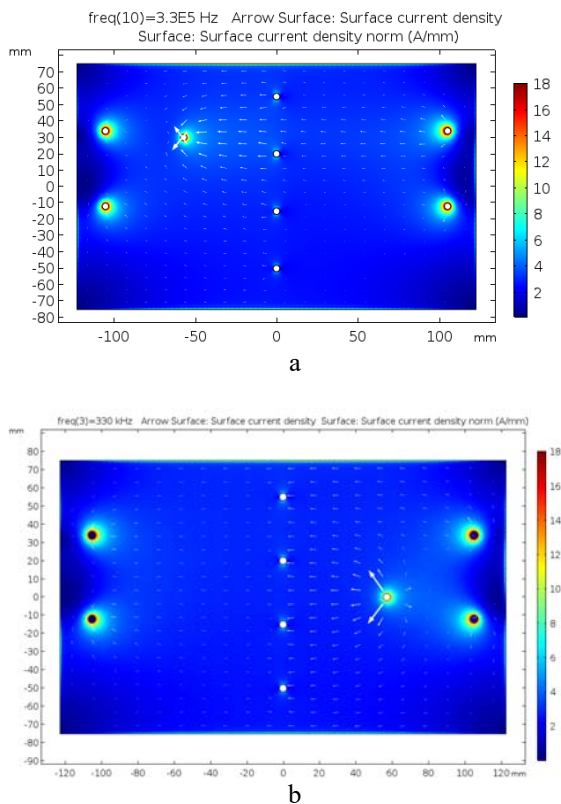


Figure 5. Plots of surface current density of top (a) and bottom (b) plates at 330 kHz.

in both cases. Accuracy of loss calculation can be estimated using Table 7.

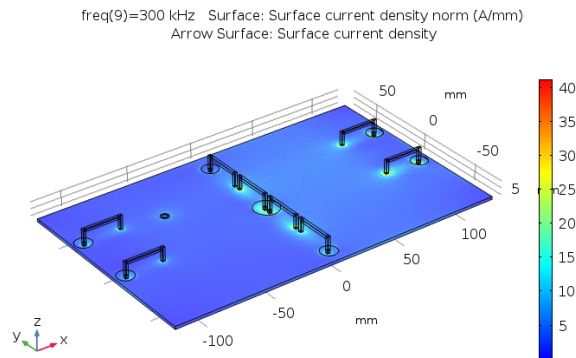


Figure 6. Current density at 300 kHz. Caps (pairs, $C=2 \times 6 \mu\text{F}$) modeled as “handles”. LE handlebar (long side) length equals to pitch=27mm.

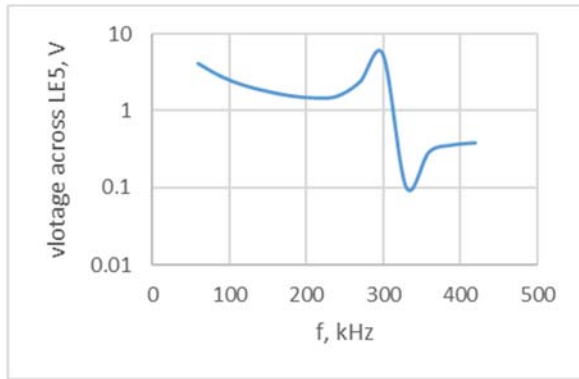


Figure 7. Voltage across LE5 vs frequency.

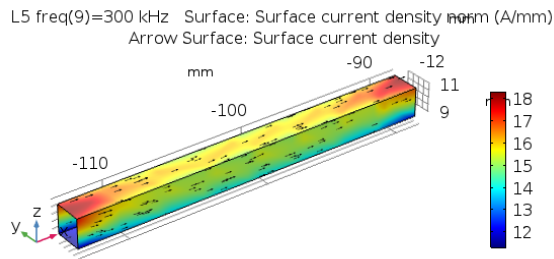


Figure 8. Surface current in LE5 at 300 kHz.

Table 4. Copper plates losses for both handlebar and dot (cylinder) capacitor models.

	handles	cylinders
freq (kHz)	Surface loss (W)	Surface loss (W)
60	3.2023	3.20
90	3.2967	3.27
120	3.5603	3.34
150	3.5744	3.39
180	3.5206	3.45
210	3.6913	3.52
240	4.215	3.59
270	8.0707	3.71
300	88.114	4.11
330	9.1919	60.73
360	4.7929	5.08
390	4.3569	4.01
420	4.2294	3.99

References

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- [3] G. Eriksson, “Efficient 3D Simulation of Thin Conducting Layers of Arbitrary Thickness”, IEEE International Conference on Electromagnetic Compatibility, Honolulu, HI, 2007, pp. 1-6.
- [4] IGBT Module FF400R12KT3, Infineon datasheet.

Acknowledgements

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5 Appendix – estimating accuracy of modeling with TBC

Here we compare TBC-based simulations to their fully-resolved volume counterparts. For simplicity and clarity, we simulate mostly in 2D, both flat (2D) and axisymmetric (2D-axi) geometries. We limit the examination to a case of Poynting vector being perpendicular to the conductor plane as pertinent to PCB simulations. As this work progressed, need in a 3D verification became evident, so we include also a paragraph on 3D simulations emulating those in 2D.

All simulations of this section are viewed in the context of an important figure of merit - ratio of copper thickness to skin depth – see Figure 9.

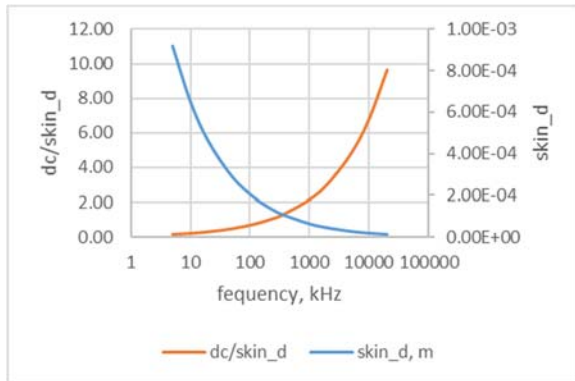


Figure 9. Skin depth, skin_d, and ratio of copper thickness, dc, to skin_d.

5.1 2D simulations

A 2D (flat) model is shown in Figure 10. All boundaries are straight. It is actually a 1D case, with dependence on y-coordinate only. (Unfortunately, Comsol does not offer an interface for magnetic fields in 1D.) A current 1 A is injected into central blue domain with copper thickness $dc=0.14$ mm Figure 10a. The other two layers with the same thickness are “passive” copper. The model is resolved for two cases. In the first, field distribution is found in volume with full account of the skin effect. In the second case, TBC is set on the boundaries closest to the central layer Figure 10b. In both cases, the same mesh is used, where the first boundary layer thickness is set at $\frac{1}{4}$ of the skin depth. Perfect Magnetic Conductor condition is set on vertical boundaries, which means that the passive layers see a planar incident wave with the Poynting vector perpendicular to these layers.

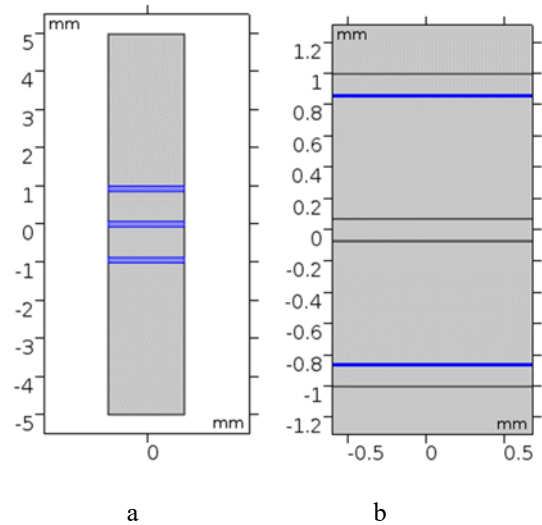


Figure 10. 2D model used for comparison of full volume (a) and TBC (b) simulations. Blue is copper. In (a), copper is in domains, whereas in (b), copper is in sheets.

A comparison of various field plots for full volume and TBC at several frequencies showed very little difference between the two cases. Also, volumetric and surface losses in a very wide frequency range differ very little. However, almost ideal match (their ratios are virtually unity! See Table 7 in continuation) raises a red flag.

A caveat might be surfaces’ curvature. Ref [2], [3] and Comsol user manuals stipulate that the layer thickness must be much smaller than the radius of curvature of the layer and the size of the layer. Although curvature does not seem much relevant to rigid PCBs, we investigate also this factor.

To this end, we roll the flat geometry of model Figure 10 into a cylinder with $OD=r_0$ which is varied from 5 to 100 mm. Only a 10-deg-sector is modeled Figure 11. Again, this is essentially a 1D model that would have only r-coordinate variation in polar coordinates.

Ratio of volumetric to surface losses is shown in Table 5. It is insensitive to r_0 , which is legitimate because r_0 is larger by two-three orders of magnitude than dc. Against expectations based on 2D modeling of straight boundaries Figure 10, this ratio is much larger than unity at low frequencies, even when r_0 is very large compared to dc. We do not have any plausible explanation to that.

We also modeled in 2D-axisymmetric approximation. Description of this modeling is omitted here for the brevity sake. However, some results are included in Table 7.

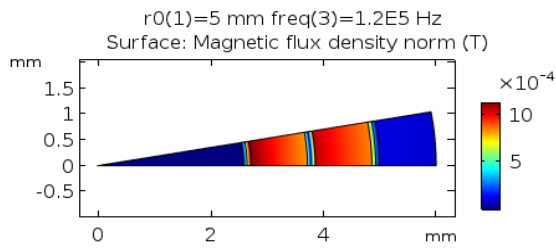


Figure 11. Copper cylindrical shell with thickness d_c carries current 1A in axial direction. It is surrounded by two copper shell with the same thickness spaced by $d_{ins}/2=1$ mm.

Table 5. 2D model of cylinder carrying axial current Figure 11. Ratio of volumetric to surface losses for a set of frequencies and r_0 .

f	r_0 , mm				
Hz	5	10	20	50	100
	Ratio of volumetric to surface losses				
20000	2.89	3.17	3.26	3.29	3.29
50000	2.07	2.09	2.09	2.09	2.09
1.20E+05	1.41	1.39	1.38	1.38	1.38
2.40E+05	1.07	1.06	1.05	1.05	1.05
3.60E+05	0.96	0.95	0.95	0.95	0.95
1.00E+06	0.97	0.97	0.96	0.96	0.96
2.00E+06	1.00	1.00	1.00	1.00	1.00
5.00E+06	1.00	1.00	1.00	1.00	1.00
1.00E+07	1.96	1.98	1.99	2.00	2.00
2.00E+07	1.96	1.98	1.99	2.00	2.00

5.2 3D simulations

3D simulations certainly seem an overkill in a case when physics is 1D. However, stark discrepancy between 2D-planar models (Figure 10) and those with curved boundaries (Figure 11) raises questions which of them, if any, are correct. Certainly, almost ideal match of volumetric and surface losses of the simplest case Figure 10 is suspicious. This is why we set a model replicating that of Figure 10 in 3D Figure 12.

A comparison of volumetric and surface losses in 3D is given in Table 6. Their ratios for 2D cases with low curvature ($r_0=100$ mm) and 3D are summarized in Table 7 which is a digest of the previous tables. There is a fair correspondence between the results except that of flat 2D which should be distrusted. The best range for using TBC according to these data is $d_c/skin_d=1\div 5$.

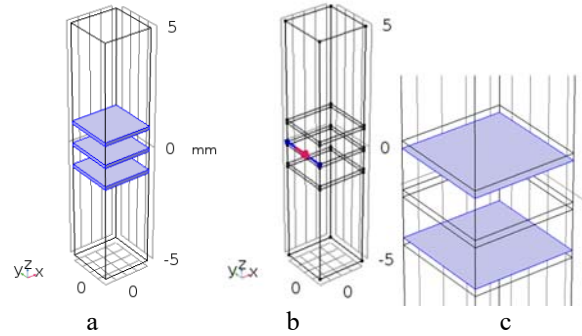


Figure 12. 3D model of three infinite copper slabs (blue), the central of which (b) carries current in y-direction. TBCs are set as shown in (c).

Table 6. Ratio of volumetric to surface losses in 3D.

freq (kHz)	skin_d, m	dc/skin_d	Vol. loss, (W)	Surface loss (W)	vol/surf
5	9.19E-04	0.15	0.19	0.05	4.27
10	6.50E-04	0.22	0.26	0.06	4.12
20	4.60E-04	0.30	0.29	0.09	3.21
50	2.91E-04	0.48	0.30	0.14	2.10
120	1.88E-04	0.75	0.31	0.22	1.39
240	1.33E-04	1.06	0.33	0.31	1.06
360	1.08E-04	1.29	0.37	0.38	0.95
1000	6.50E-05	2.15	0.62	0.64	0.96
2000	4.60E-05	3.05	0.91	0.91	1.00
5000	2.91E-05	4.82	1.43	1.43	1.00
10000	2.06E-05	6.81	2.03	1.01	2.00
20000	1.45E-05	9.63	2.88	1.43	2.01

Table 7. Summary: Ratio of volumetric to surface losses in 2D and 3D.

freq (Hz)	dc/skin_d	sector, r0=100mm	cylinder, r0=100m	3D	flat 2D
5000	0.15	6.53	6.64	4.27	0.98
10000	0.22	4.64	4.70	4.12	0.99
20000	0.30	3.29	3.33	3.21	1.00
50000	0.48	2.09	2.11	2.10	1.00
1.20E+05	0.75	1.38	1.39	1.39	1.00
2.40E+05	1.06	1.05	1.06	1.06	1.00
3.60E+05	1.29	0.95	0.96	0.95	1.00
1.00E+06	2.15	0.96	0.98	0.96	1.00
2.00E+06	3.05	1.00	1.02	1.00	1.00
5.00E+06	4.82	1.00	1.01	1.00	1.00
1.00E+07	6.81	2.00	2.03	2.00	1.00
2.00E+07	9.63	2.00	2.04	2.01	1.00