Simple Disk Piezo Transformer based Oscillator

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Abstract: In this contribution we present the development steps of a disk piezoelectric ceramic transformer (D-PT) using COMSOL Multiphysics. The use of this software turned out to be a very valuable tool to find good positions for the D-PT clamping points, as well as to determine the essential electrical characteristics under various operating conditions. Furthermore, the coupling of a D-PT with a bipolar NPN transistor to form an auto-oscillator was simulated and practically realized. The comparison between the simulations and the measurements made on our prototype are found to be in good agreement.

Keywords: Piezo transformer, Step-Up Voltage ratio, Efficiency, Oscillator, Bipolar transistor.

1. Introduction

The piezoelectric transformer (PT) was first realized by C. A. Rosen back in 1956. The coupling effect between the electrical and mechanical energy is used to produce voltage step-up or step-down, galvanic isolation, balanced input/output voltage etc. Moreover, the PT can replace the magnetic transformer in many applications such:

- To power the cold cathode fluorescent lamp of the LCD-TV backlight.
- Charge generation for high-voltage low-power application.
- Very low power high efficiency DC/DC converter.
- Battery chargers for mobile phones, ac/dc adapters for mobile computers.
- Step-up / step down conversion in high magnetic field environment (IRM).

The main advantages of PTs are the weight and the size reduction in low power applications while guarantying low EMI.

Having at our disposal a large number of homogenously poled disks, we decided to build and to investigate the performances of D-PT. It is worth mentioning that the D-PTs require only a single poling process, thus reducing the complexity and the cost of producing them. From the many data found in the literature survey [1], the ring-dot type was selected.

This paper is organized as follows: In section 2, the basic simulation parameters are shown as well as simulation results in a "no clamping" condition. In the next section, the clamping points positions are determined as well as their resulting effect on the D-PT efficiency. Experimental results are shown in section 4. Section 5 presents the simulations and the implementation of a simple D-PT based bipolar transistor oscillator whereas the last section concludes this work.

2. Basic Simulation Parameters

The first simulation step consists in the modelling of the Piezo transformer without any clamping point. The two next physics are used for the frequency domain analysis: "Piezoelectric Devices" (pzd) and "Electrical Circuit" (cir). The geometry dimensions of the **PZT-5H** Piezo disk used in our work are the following: External diameter **8 mm**; internal diameter **2mm** and thickness **300μm**.
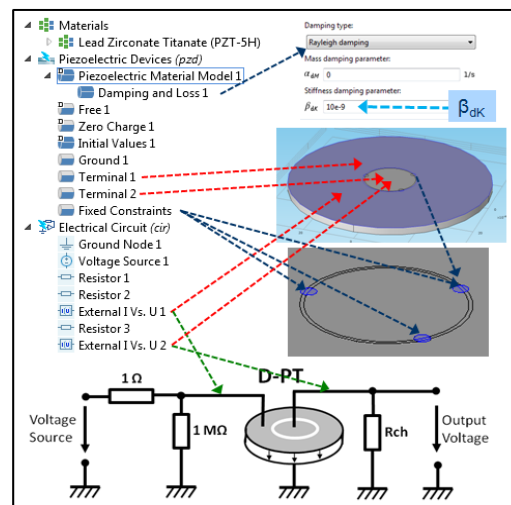

Figure 1. Basic simulation parameters settings.

We also set the Piezo damping settings to "Rayleigh damping" with a starting value of $\alpha=0$, $\beta= 5\cdot10^{-9}$, a value that would later be readjusted based on our measurements. It is worth mentioning that this type of damping is selected since it applies to both "Frequency domain" and "Time dependant" analysis. Fig. 1 shows the setting of some key parameters.

In Fig. 2 both the voltage step-up ratio (Gv) and the efficiency (η) are displayed versus frequency in the "no clamping" condition.
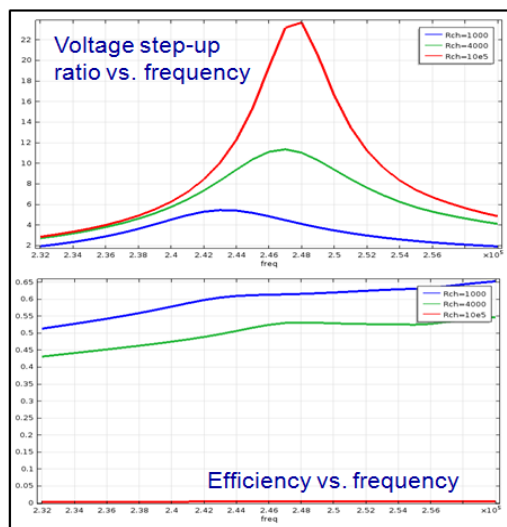
Figure 2. No clamping: Gv(f) and η(f)

3. Clamping Position Determination

In the second step of simulation, the D-PT clamping points positions are determined from the displacement plots. The following conditions must be simultaneously satisfied:

- A voltage step-up ratio of at least 10 under a few k-ohms of load at the optimum frequency of operation.
- A D-PT damping limited as much as possible so as to maintain the efficiency to an acceptable level.
- Mechanical clamping points and electrical contacts practicable for an industrial product.

In Fig. 3 we can see the D-PT with its clamping pins and Fig. 4 displays a 3D plot of the displacement simulation. Then, from the measurements made (section 4) on identical prototypes, the "Rayleigh damping is readjusted to $\beta=10\cdot10^{-9}$. Fig. 5 shows both Gv(f) and η(f).
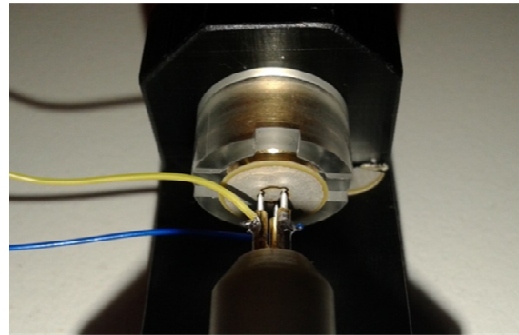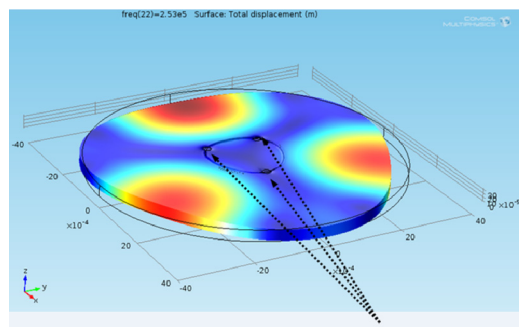

Figure 3. D-PT with its clamping pins

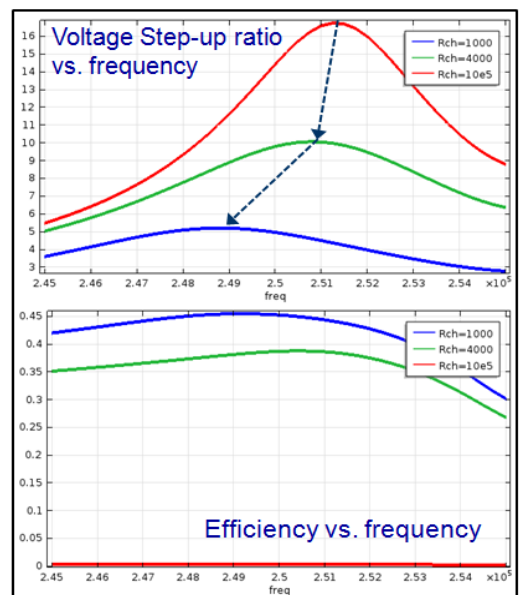**Figure 4**. Displacement example with the 3 clamping points

Figure 5. Gv(f) and η(f) with three clamping points

Next the position of the clamping points is changed. From the many simulations done bringing the points closer from the disk center improves both Gv and η (Fig. 6). However, that makes the practical realization much harder to

assemble reliably; thus we will keep these three points at the boundary between the input/output terminal surfaces.
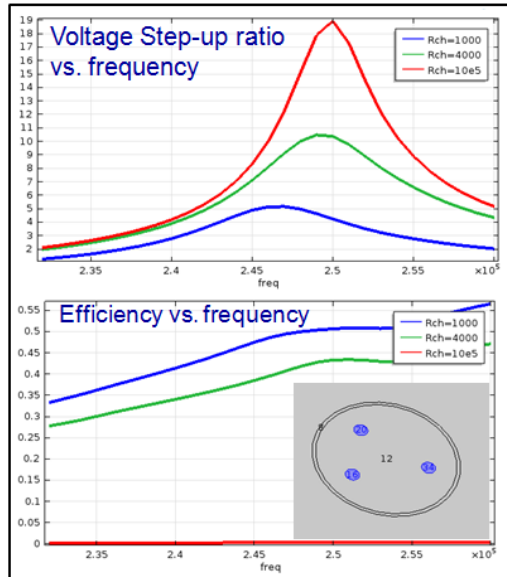

Figure 6. Clamping closer from the disk center.

4. Experimental Results

Fig. 7 and 8 present the D-PT with its clamping pins as realized in our lab.

Figure 7. D-PT bottom holder.

A special care was placed upon loading the disk Piezo element surface as little as possible; thus maintaining an acceptable efficiency. The following values are computed efficiencies from the measurements with two different loads R_L:

$R_L = 1\ K\Omega$ Input: 2 Vpp, 125 mApp, 20^0 of phase
Output: 10Vpp   ➔ **η = 51%**   *Simulation: 45%*

$R_L = 3.9\ K\Omega$ Input: 2 Vpp, 160mApp, no phase shift
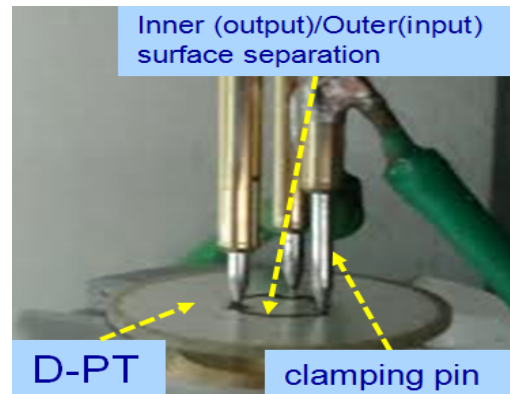Output: 20Vpp   ➔ **η =42%**   *Simulation: 38%*

Figure 8. D-PT clamped between 3 movable pins and 3 fixed poles (at the bottom).

Furthermore, the next figure shows the good agreement between the measurements and the simulations of Gv(f) for three different loads (the scales are identical for both the measurements and the simulations).
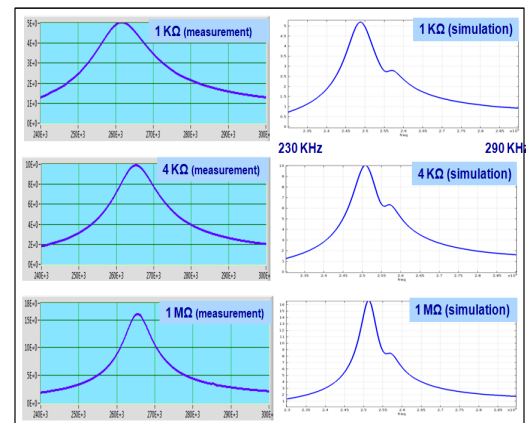

Figure 9. Gv(f), with f: 230 KHz ➔ 290 KHz

5. Simple D-PT based Oscillator

Finally, a third simulation step consisted in a "Time domain" analysis to confirm our laboratory measurements of our D-PT bipolar NPN transistor oscillator. Due to the low D-PT input impedance, we used a common collector configuration (Fig. 10). The results of the simulation validate the fact that with this simple schematic the running frequency is 20% higher than the optimal frequency of the D-PT running alone. The measured frequency of oscillation was around of 320 KHz. The minimum supply voltage was 2V.

A careful analysis of the D-PT input-output phase as well as its input impedance (Fig. 12) as generated by the simulation gives the clue as to why there is such a frequency difference.
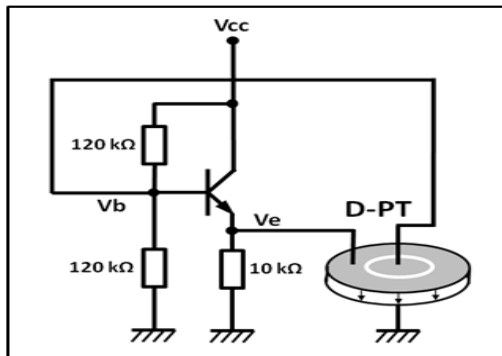

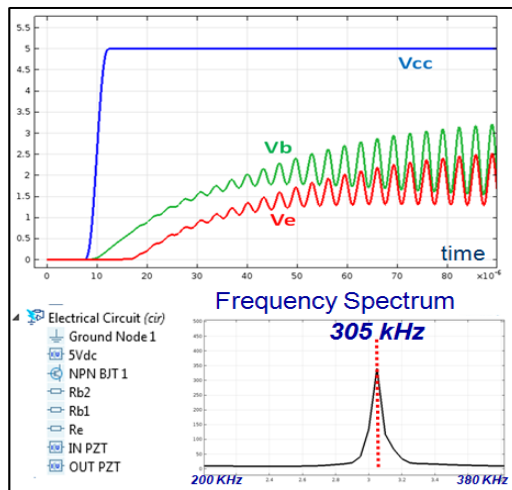**Figure 10**. Oscillator Electronics Schematic

Figure 11.   Simulation results

Specifically, from the ***Output-Input Phase*** plot it is obvious that the most likely oscillation frequency will occur when the phase is the closest from 0 degree, i.e. near 304 kHz. Note that the D-PT ***Input Impedance Module*** loads only marginally the D-PT output through the emitter/base junction, thus an Rch of 40 KΩ is a realistic assumption!

6. Conclusions

In conclusion, the use of COMSOL Multiphysics turned out to be a very effective way to find good locations for the D-PT clamping points, a particular challenging issue
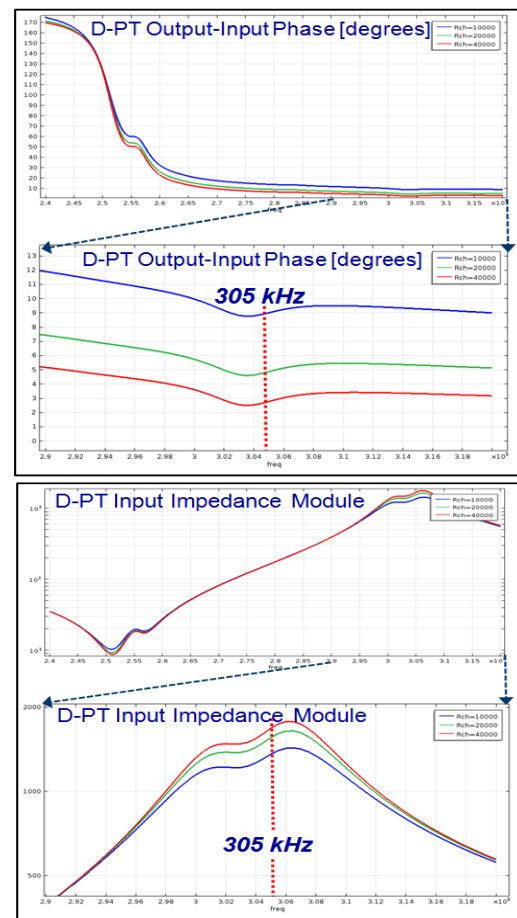

Figure 12. $\Phi_{OUT}(f)$–$\Phi_{IN}(f)$, $Z_{IN}(f)$

with such a light weight device. Moreover, the coupling of "pzd" with "cir" gives the key electrical parameters (e.g. input impedance, efficiency....), the influence of the device geometry and of the clamping positions upon them.

9. References

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2. Yang S.-L., Chen S.-M., Tsai C.-C., Hong C.-S., Chu S.-Y., Fabrication of High-Power Piezoelectric Transformers Using Lead-Free Ceramics for Application in Electronic Ballasts, *IEEE Trans. on UFFC*, **VOL. 60**, p408-413 (2013)